Edge & Cloud Systems based on Open Standards

Manolis Marazakis (FORTH)

Perspectives from the RISER and HIGHER Projects

ML4ECS workshop - HiPEAC'26

European Commission
Horizon Europe
2021-2027

26th of January, 2026

Motivation for this talk

Why Edge & Cloud system platforms ?

- Market relevance and deployment scale
- Strategic positioning in the computing continuum
- Economic sustainability
- Complementarity with HPC investments

[personal position statement]
Edge & Cloud platforms represent where EU technology must compete to be relevant, while open standards represent how the EU can realistically compete, given a fragmented industrial base and late entry compared to established non-EU competitors.

Open standards enable collaboration rather than duplication, pooling limited European resources toward interoperable solutions rather than incompatible proprietary efforts.

Why Open standards ?

- Avoid vendor lock-in & single points of failure
- Ecosystem building and interoperability
- Lowering barriers to entry
- Software ecosystem leverage
- Transparency and security
- Long-term resilience

+ EU's digital sovereignty and strategic autonomy

In this talk: Highlights from two Research & Innovation projects (RISER, HIGHER) active in this area. Facts & Plans intermingled with personal views … Trust but verify ☺

Can we design and build Edge & Cloud system platforms based on open standards in Europe today?

Project Mission Statement

Can we design and build Edge & Cloud system platforms based on open standards in Europe today?

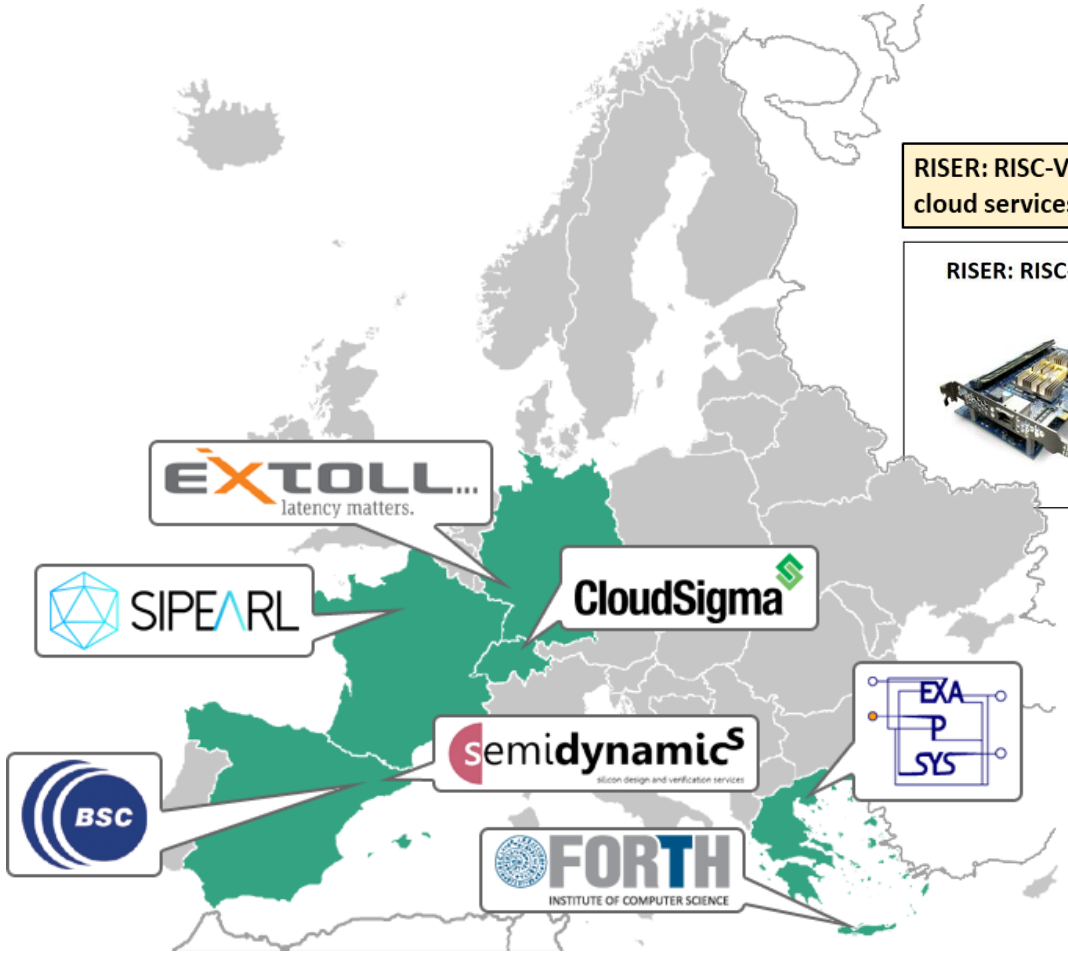
Open standards for ISA == RISC-V

+ Arm ISA (sovereignty-focused projects funded by EuroHPC Joint Undertaking, mainly for HPC)

+ Cloud infrastructure roadmap

RISER in a nutshell

https://zenodo.org/communities/riser/records



RISER: RISC-V based Linux server for cloud services, built on open interfaces

RISER: RISC-V for Cloud Services

RISC-V Processors
Source: EPI and EUPilot projects (chips)
* Currently operating on system boards designed for dev/test purposes

Server Boards (PCB + firmware)
Standard form factors (PCIe accelerator card, Microserver)
* Following industry standards to utilize server I/O peripherals

- DRAM Memory
- NVM-Express Storage
- 100 Gbps Ethernet

Boot Firmware
Initialization of execution platform, Including high-speed I/O peripherals (storage, networking)

OS, drivers, runtime
Configured/adapted for cloud services: workload acceleration, networked storage, containerized execution
*Integration in IaaS environment

https://riser-project.eu

https://www.linkedin.com/company/riser-project/

https://twitter.com/RiserProject

Integrated all-European Hardware and Open-Source Software for Cloud Services and Applications

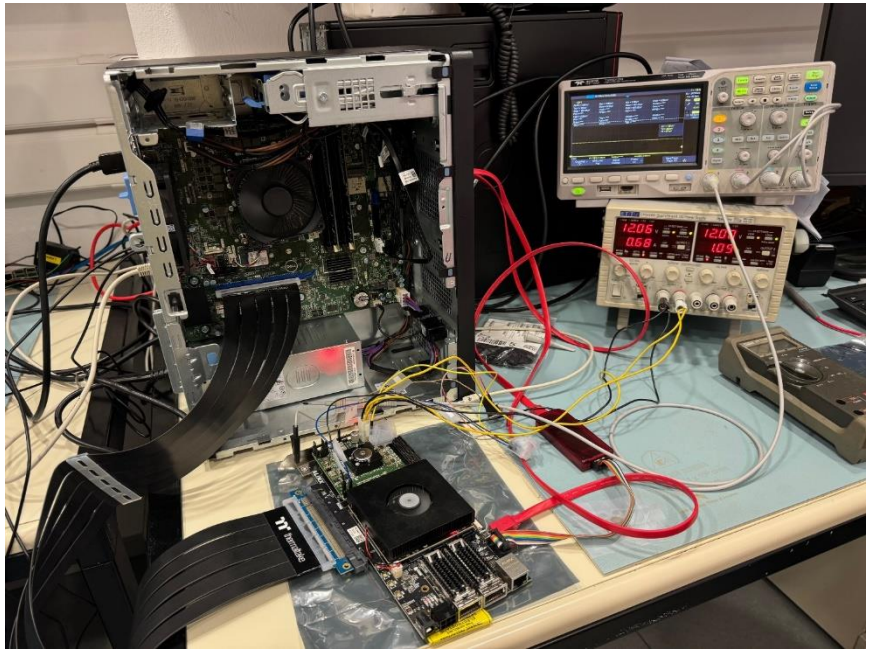
[RIA Project started on Jan. 1, 2023]

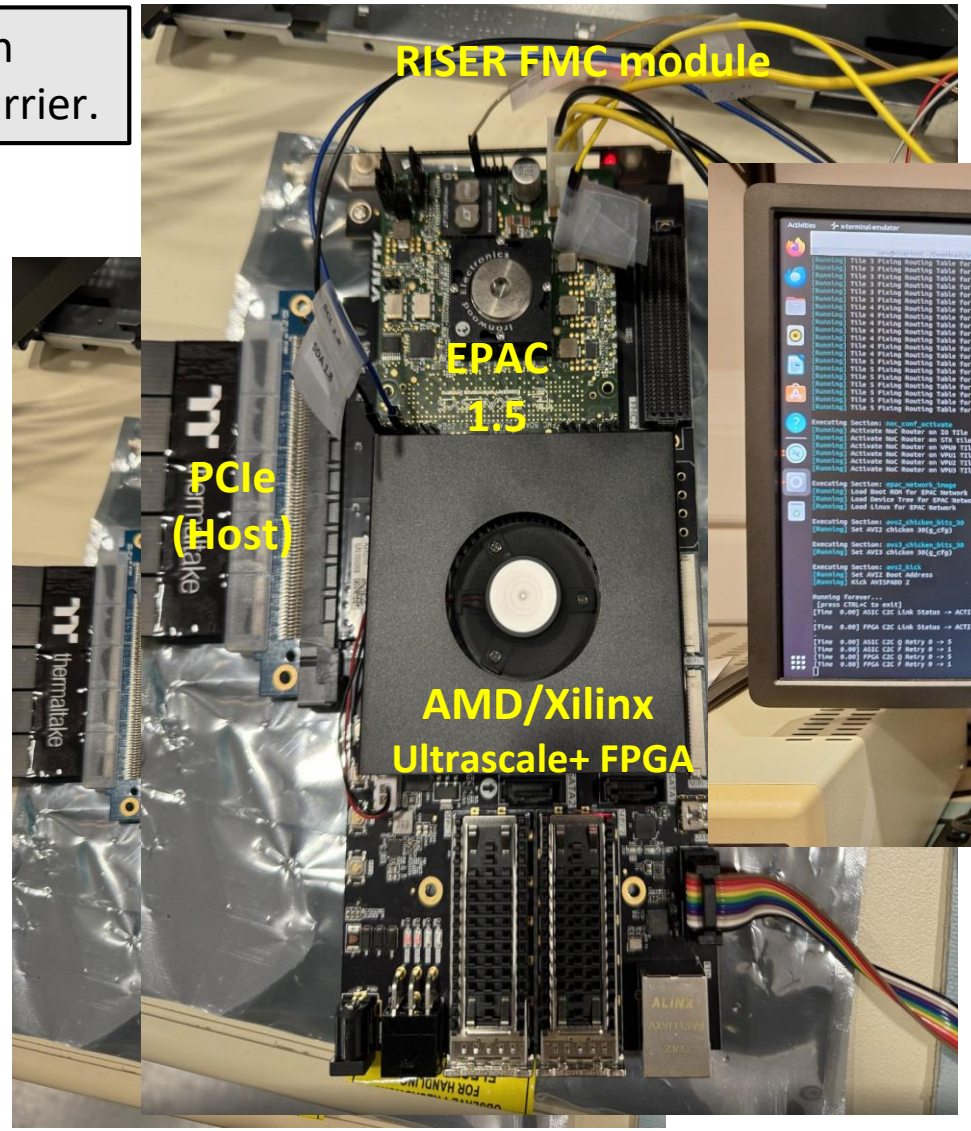
Results

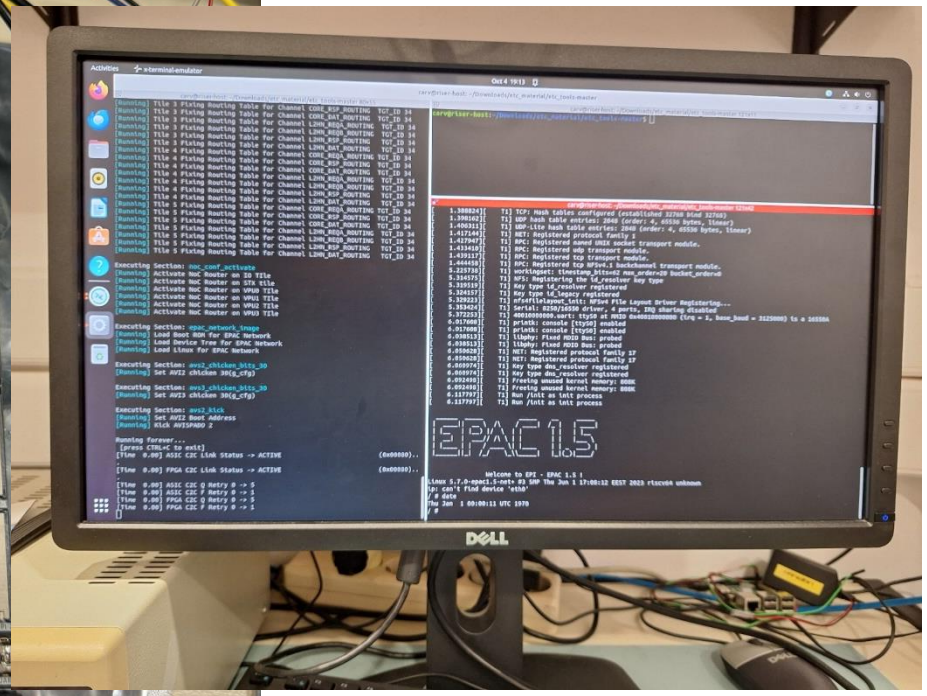
- **Chips from the EPI project → basis of platform prototypes**
  - **Host-Accelerator**
    - **Host: Arm HPC SoC, by SiPEARL**
    - **Accelerator: RISC-V SoC, with the Avispado core by Semidynamics**
  - **Microserver**
    - **Standalone (FPGA-assisted), using RISC-V SoC**
    - **upcoming: variant based RISC-V SoC from the EUPILOT project**
- **Open-source designs, incl. Firmware, OS, runtimes**
- **Use cases:**
  - **Acceleration: OpenMP multi-device task offload**
  - **Cloud: Containers & Orchestration (Kubernetes) runtime, IaaS, Networked Storage**

Prototype using test-chip from EPI

PCIe-hosted Accelerator: test-chip hosted on miniaturized FMC daughtercard on FPGA carrier.





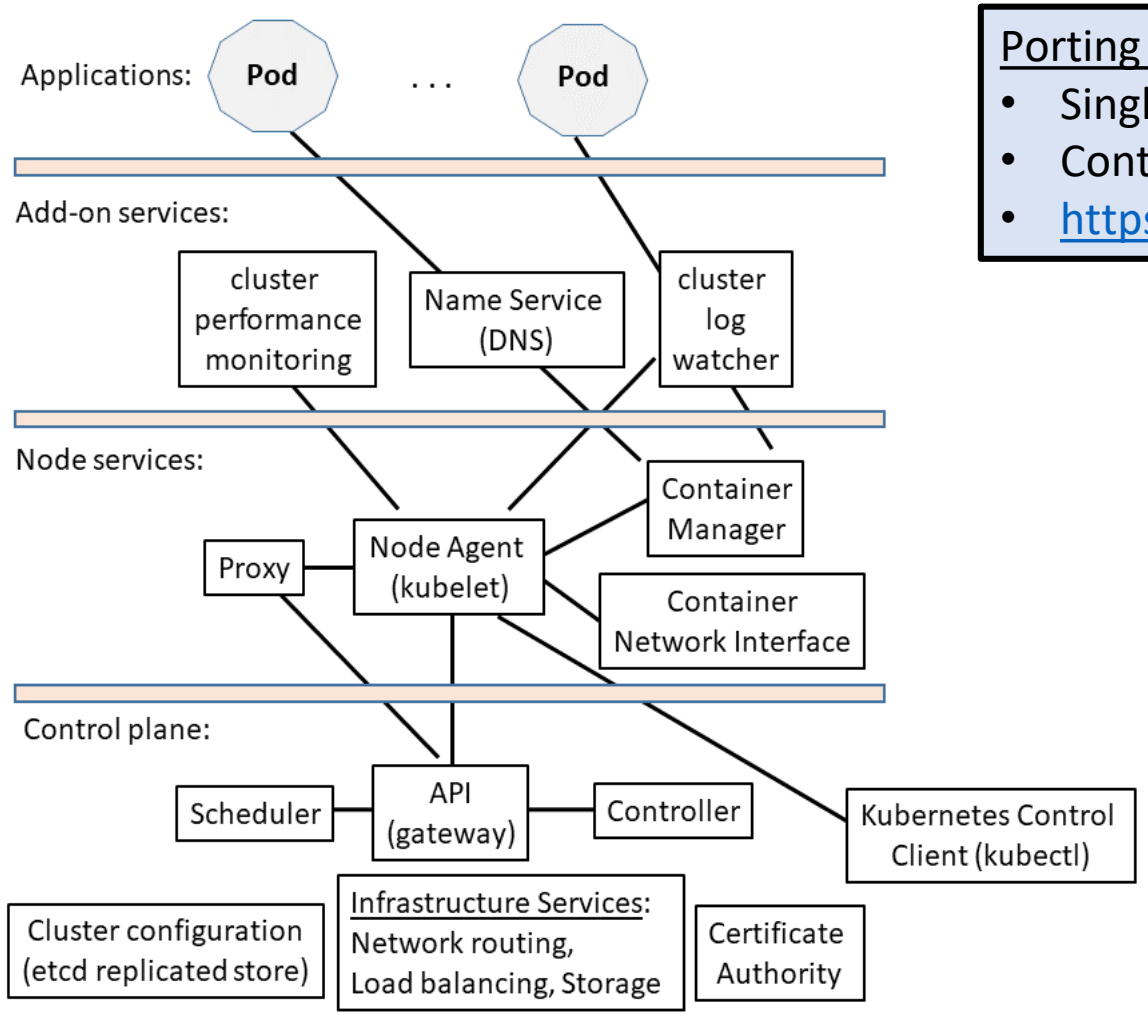


Ongoing effort:
(i) Host+Accelerator (task offload)
(ii) Microserver (self-hosted, I/O)

Open Access Programme (Q4/2026)

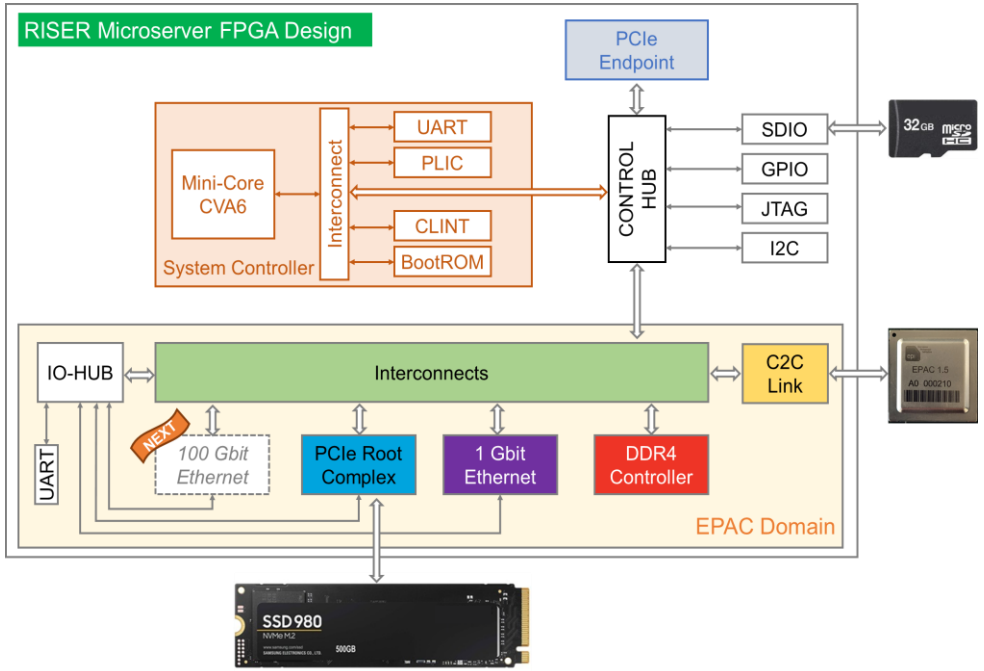
Microserver: Container Services

Container runtime & orchestration: Infrastructure & Node Services, Control Plane



Porting the K3S Kubernetes distribution to RISC-V

- Single binary for essential Kubernetes services, for easier deployment
- Contributions (PRs) to upstream open-source projects
- https://github.com/CARV-ICS-FORTH/kubernetes-riscv64



Are we there yet ?

High-end chips are HARD. Schedules and Supply Chains are complex.

Design + Verification + Integration …

- Accelerators

Gaps in availability and integration of suitable IP blocks (incl. Host + Accelerator interaction support, via open-standard HW and SW interfaces)

- Servers

Gaps in availability and integration of suitable IP blocks (incl. efficient use of high-speed I/O peripherals, and open-standard fully-featured SW stacks operating in actual Data Center setting)

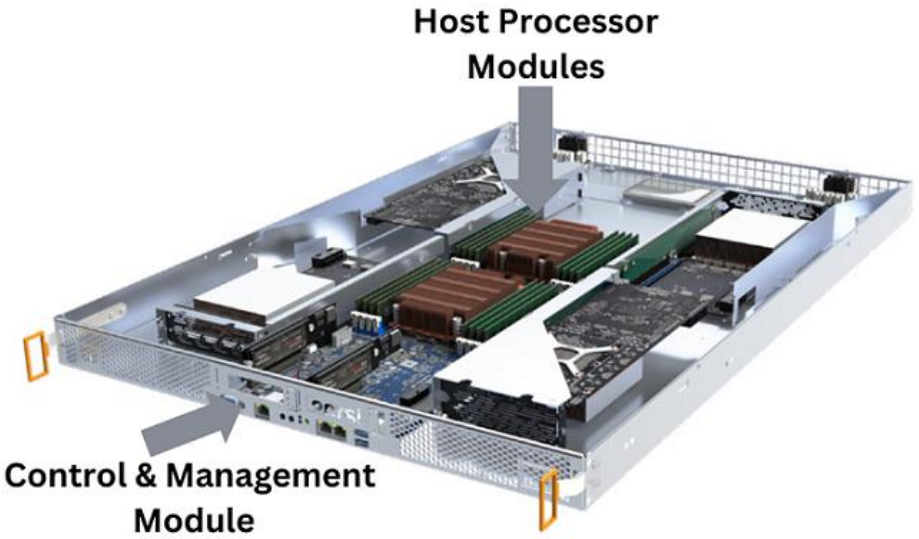
My personal view is a _qualified_ but confident YES.

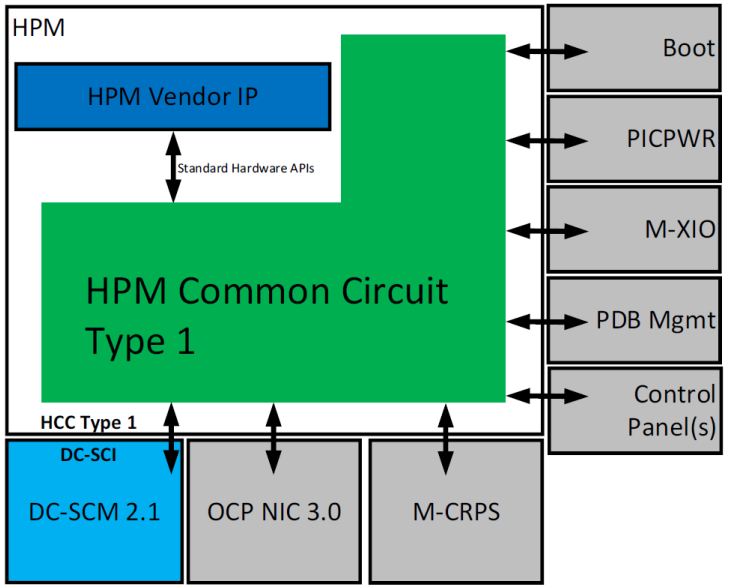
→ We should also have a roadmap for advanced DC systems as well !

HIGHER (RISER's continuation)

European Heterogeneous Cloud/Edge Infrastructures for Next Generation Hybrid Services

- **Open Compute Project → "recipes" for data-centre systems**
- **HIGHER -> Data-centre ready processor (Arm, RISC-V) & management modules based on OCP (HPM, DC-SCM)**



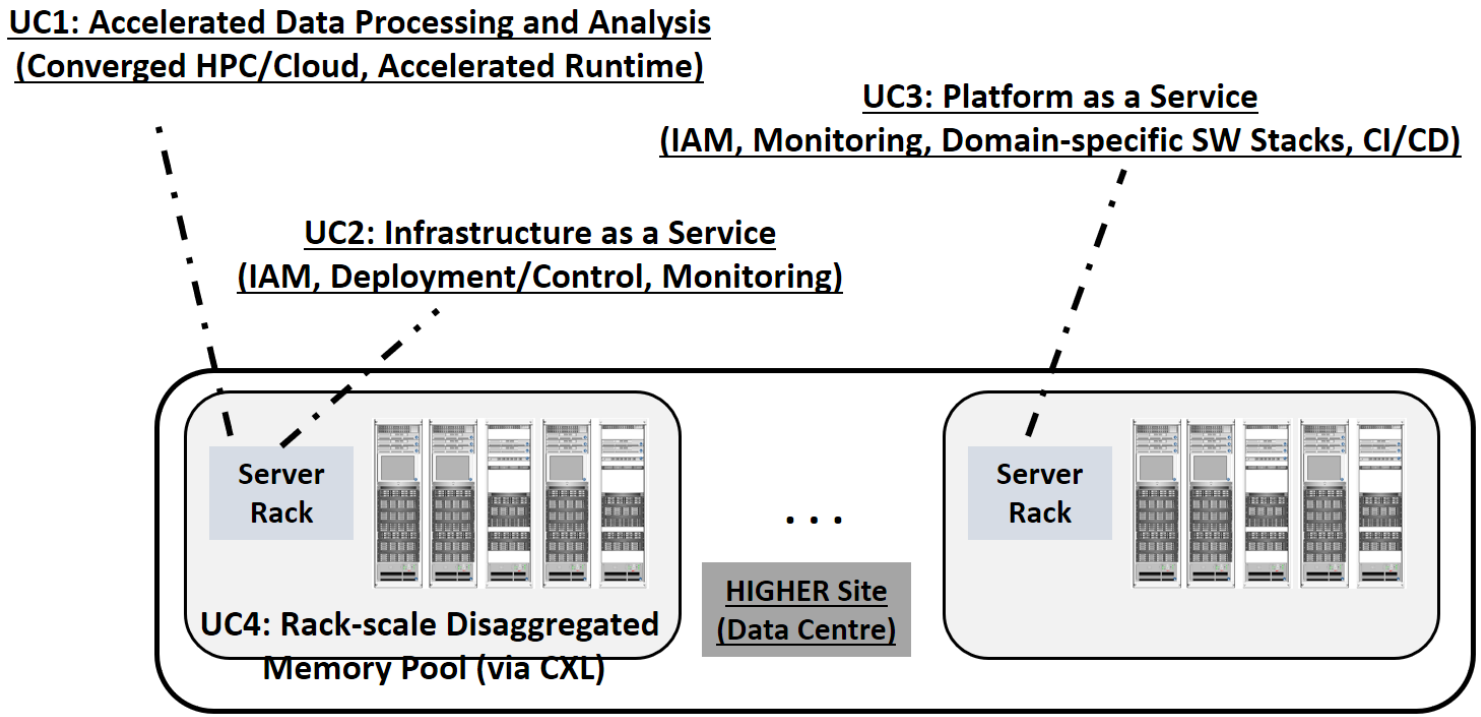


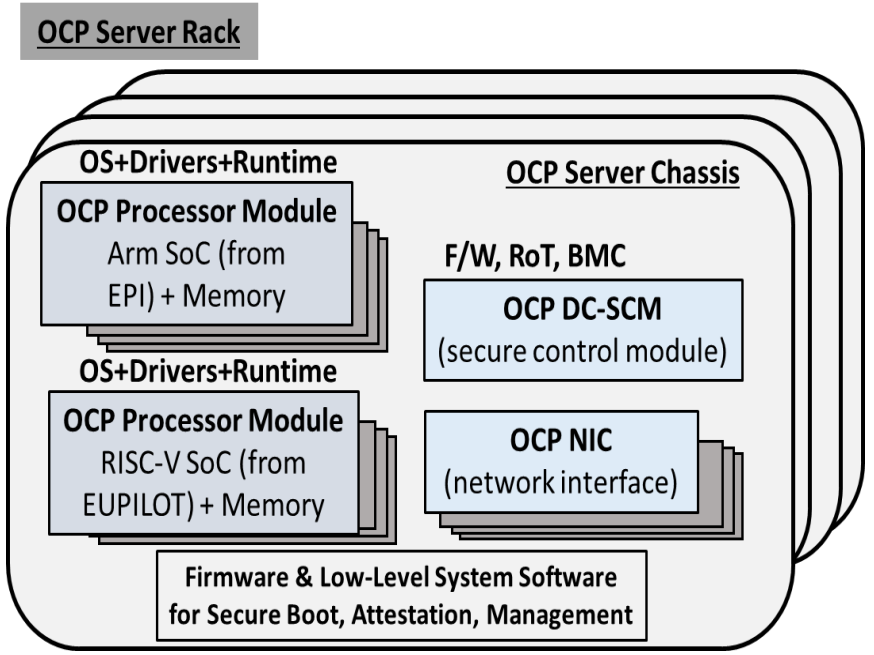
Key themes: Cloud, Edge, ARM, RISC-V, Computing Continuum, Computing for servers, data centres, Open Source Software

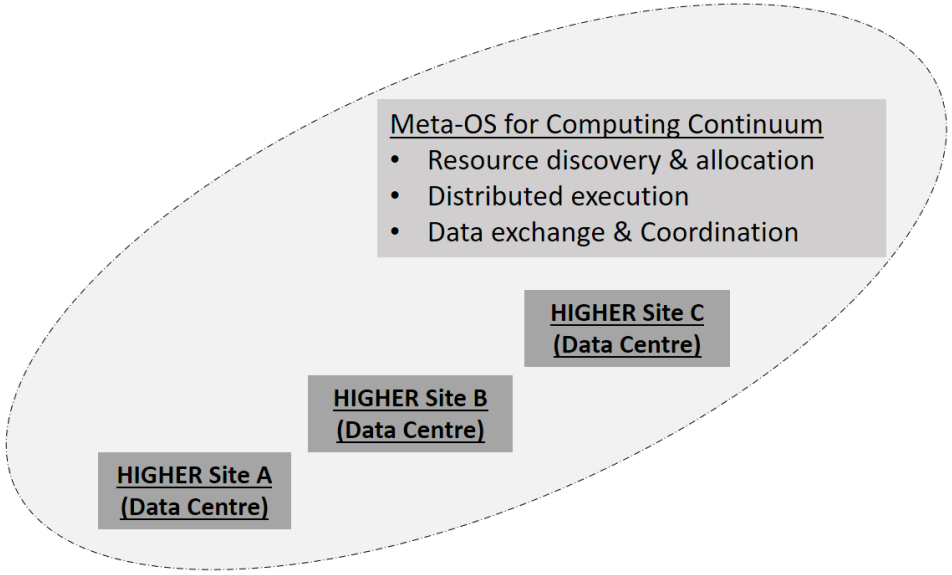
HIGHER (GA 101189612 / DG/Agency: HADEA): https://higher-project.eu

[RIA Project started on Jan. 1, 2025]

HIGHER in a nutshell



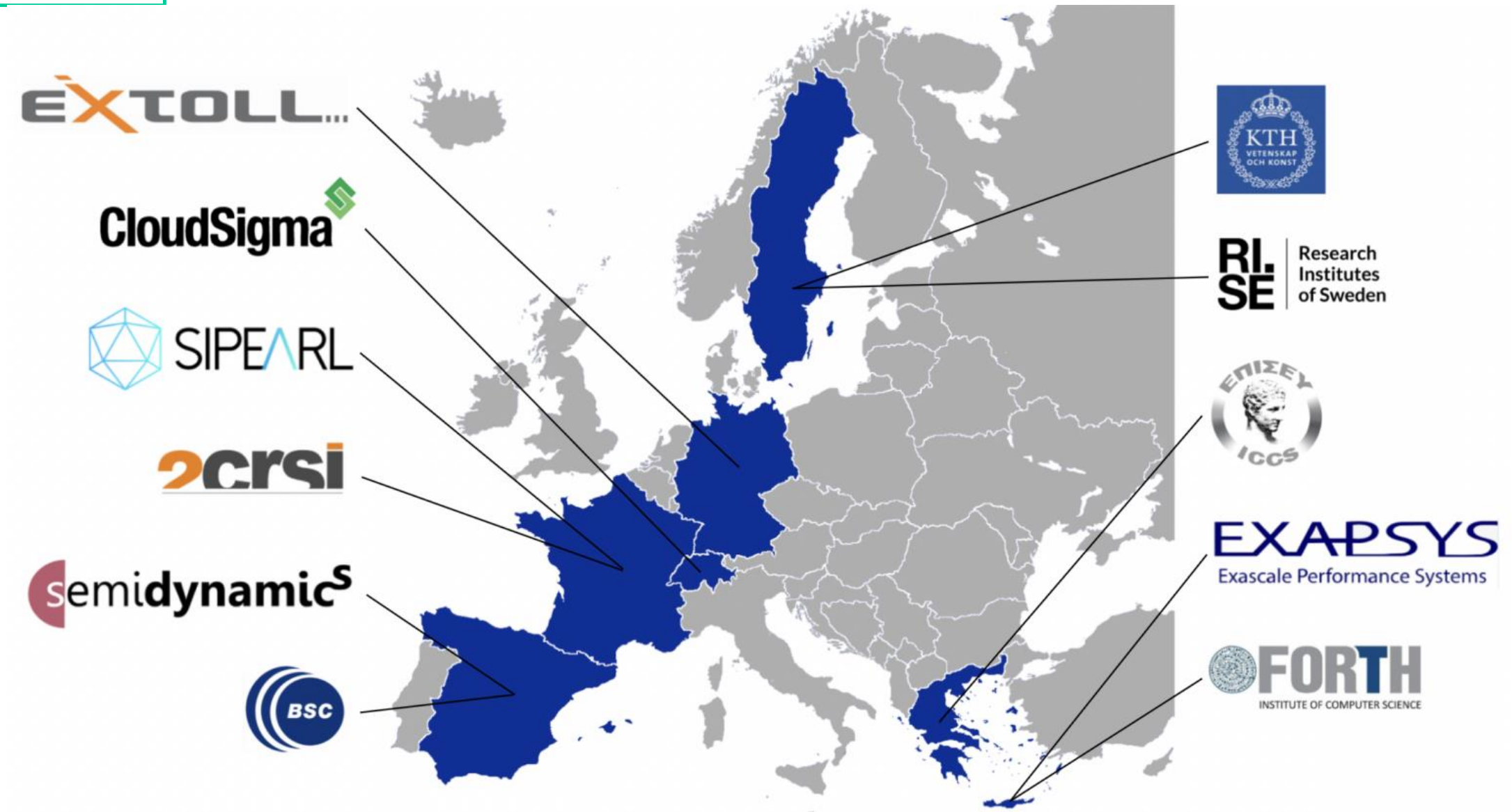




Objectives:

- ❑ Development of open-source cloud and edge HW and SW modules based on European Technologies, enabling and demonstrating full computing infrastructure deployments.
- ❑ Processing and Energy Efficiency able to satisfy the needs of demanding cloud and edge applications.

HIGHER consortium := RISER + 4



Closing remarks

- RISER has shown that a RISC-V-based Linux server for cloud services is achievable with European technology.
- HIGHER takes this further by targeting OCP-compliant data center modules—both Arm-based using SiPEARL's Rhea and RISC-V-based using EUPILOT silicon.

- High-end chips are hard. Schedules slip. Supply chains are complex. We should not underestimate the difficulty of what remains.

- **IMHO** : *The question is whether we can sustain the commitment to see it through to production-ready, commercially viable systems.*

Thank you for your attention

Disclaimer:

"Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the European Health and Digital Executive Agency (HaDEA). Neither the European Union nor the granting authority can be held responsible for them."

European Commission
Horizon Europe
2021-2027

RISER: https://riser-project.eu
HIGHER: https://higher-project.eu